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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: Confirmation No.: 3437

NISHIKAWA et al. Art Unit: 2811

Serial No.: 10/786,296 Examiner: O. Nadav

Filed: February 26, 2004 Docket No.: 103213-00072

For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE CONFIGURED TO PREVENT THE GENERATION OF A REVERSE CURRENT IN A MOS TRANSISTOR **(AS AMENDED)**

AMENDMENT UNDER 37 C.F.R. § 1.111

Introductory Comments

Director of the U.S. PTO
P.O. Box 1450
Alexandria, Virginia 22313-1450

December 21, 2004

Sir:

In response to the Office Action dated September 23, 2004, please amend the above-titled application as follows: